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1 Software for Reconfigurable Systems: Incremental reconfiguration of multi-FPGA systems

K. K. Lee, D. F. Wong

February 2002 **Proceedings of the 2002 ACM/SIGDA tenth international symposium on Field-programmable gate arrays**

Publisher: ACM Press

Full text available: pdf(146.68 KB) Additional Information: full citation, abstract, references

In reconfigurable computing, circuits implemented on multi-FPGA systems have to be incrementally modified. Since reconfiguring an FPGA is time-consuming, the time for reconfiguration depends on the number of FPGAs to be reconfigured. Our objective is to reduce the number of such FPGAs. In this paper, we consider the specific problem of incrementally reconfiguring a multi-FPGA system that utilizes the direct interconnection architecture, where routing connections between FPGAs are to neighbors th ...

2 Target architecture oriented high-level synthesis for multi-FPGA based emulation

Oliver Bringmann, Carsten Menn, Wolfgang Rosenstiel

January 2000 **Proceedings of the conference on Design, automation and test in Europe**

Publisher: ACM Press

Full text available: pdf(122.87 KB) Publisher Site Additional Information: full citation, references, index terms

3 Multi-terminal net routing for partial crossbar-based multi-FPGA systems

Abdel Ejnioui, N. Ranganathan

February 1999 **Proceedings of the 1999 ACM/SIGDA seventh international symposium on Field programmable gate arrays**

Publisher: ACM Press

Full text available: pdf(1.06 MB) Additional Information: full citation, references, citings, index terms

Keywords: FPGA architecture, FPGA routing, branch-and-price, integer programming, interconnect optimization, layout synthesis

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1 A Complete Network-On-Chip Emulation Framework

N. Genko, D. Atienza, G. De Micheli, J. M. Mendias, R. Hermida, F. Catthoor

March 2005 **Proceedings of the conference on Design, Automation and Test in Europe - Volume 1**

Publisher: IEEE Computer Society

Full text available: pdf(257.92 KB) Additional Information: full citation, abstract

Current Systems-On-Chip (SoC) execute applications that demand extensive parallel processing. Networks-On-Chip (NoC) provide a structured way of realizing interconnections on silicon, and obviate the limitations of bus-based solution. NoCs can have regular or ad hoc topologies, and functional validation is essential to assess their correctness and performance. In this paper, we present a flexible emulation environment implemented on an FPGA that is suitable to explore, evaluate and compare a wid ...

2 Balancing performance and flexibility with hardware support for network architectures

Ilija Hadžić, Jonathan M. Smith

November 2003 **ACM Transactions on Computer Systems (TOCS)**, Volume 21 Issue 4

Publisher: ACM Press

Full text available: pdf(719.03 KB) Additional Information: full citation, abstract, references, index terms

The goals of performance and flexibility are often at odds in the design of network systems. The tension is common enough to justify an architectural solution, rather than a set of context-specific solutions. The Programmable Protocol Processing Pipeline (P4) design uses programmable hardware to selectively accelerate protocol processing functions. A set of field-programmable gate arrays (FPGAs) and an associated library of network processing modules implemented in hardware are augmented with so ...

Keywords: FPGA, P4, computer networking, flexibility, hardware, performance, programmable logic devices, programmable networks, protocol processing

3 Wireless home networks: Design and implementation of the HiperLan/2 protocol

E. P. Vasilakopoulou, G. E. Karastergios, G. D. Papadopoulos

April 2003 **ACM SIGMOBILE Mobile Computing and Communications Review**, Volume 7 Issue 2

Publisher: ACM Press

Full text available: pdf(1.50 MB) Additional Information: full citation, abstract, references

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